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NEW PATENT APPLICATION

TITLE: SEMICONDUCTOR PACKAGE AND METHOD FOR FABRICATING THE SAME

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SEMICONDUCTOR PACKAGE AND METHOD FOR FABRICATING THE SAME

FIELD OF THE INVENTION

The present invention relates to semiconductor packages and methods for fabricating the same, and more particularly, to a semiconductor package and a method for fabricating the same, in which resin flash can be prevented from occurrence in a BGA (ball grid array) semiconductor package.

BACKGROUND OF THE INVENTION

A ball grid array (BGA) semiconductor package employs advanced semiconductor packaging technology, in which a substrate has a front side for mounting a semiconductor chip thereon and a back side for disposing a plurality of solder balls thereon, so as to provide high density of I/O connections, and to bond and electrically connect the semiconductor package to an external printed circuit board.

A flip chip ball grid array (FCBGA) semiconductor package is an improved BGA semiconductor package, wherein the semiconductor chip is bonded in an upside down manner to the front side of the substrate via a plurality of solder bumps, and is electrically connected to external devices, thereby making the overall packaging size further reduced.

However, after the semiconductor chip is placed in position on the substrate, a cavity (hereinafter called "undercavity") is formed between the semiconductor chip and the substrate at intervals between the adjacent solder bumps. If this undercavity is not filled with an insulative material, due to the difference in coefficient of thermal expansion (CTE) between the chip and the substrate, during a temperature cycle in subsequent processes, the chip and the substrate respectively suffer different thermal stress, thereby easily resulting in structural cracks or electricity loss. Therefore, in such a FCBGA semiconductor package, a flip chip underfilling process is necessarily

performed to fill the undercavity with an insulative material such as epoxy resin, so as to strengthening the semiconductor structure.

The flip chip underfilling technology has been disclosed in U.S. Patent No. 5,535,101 titled as "Leadless Integrated Circuit Package" and in U.S. Patent No. 5,218,234 titled as "Semiconductor Device with Controlled Spread Polymeric Underfill". However, this technology has the following drawbacks. First, it is time-consuming. In such a flip chip underfilling process, the insulative material is filled in a capillary filling manner around the chip; thus, the material filling is often too slow with voids easily being formed. Further, as recited in "Encapsulants Used in Flip-Chip Package" by Suryanarayna et al, the filling time is reported to be proportional to the square of the chip length; as the size of the chip increases, the filling time is prolonged, thereby making the yield further reduced. Besides, an ideal underfilling material is characterized with good fluidity and wettability, and in order to avoid improper thermal stress generated from the underfilling material against the solder bumps, a solid filler is usually added to the underfilling material, making the underfilling material with the solid filler more similar in CTE to the solder bumps. However, the addition of the solid filler greatly increases the viscosity and cost of the underfilling material.

U.S. Patent No. 6,038,136 discloses a molded underfilling technology. As shown in Fig. 1, a FCBGA semiconductor package 1 comprises a substrate 10 having a front surface 100 and a back surface 101, wherein a chip bonding area 102 is pre-defined on the front surface 100 of the substrate 10; a semiconductor chip 12 reflowed on the chip bonding area 102 of the substrate 10 in flip-chip manner via a plurality of solder bumps 11; a solder mask 16 for covering the back surface 101 of the substrate 10 in a manner as to expose a plurality of ball pads 18, which are implanted with a plurality of solder balls (not shown) thereon; and a particular encapsulating material 19 for